What Is Claimed Is:

1. A method of manufacturing copper interconnects on a semiconductor wafer comprising:

forming a layer of patterned dielectric material, said patterned dielectric material defining spaces for said copper interconnects;

depositing a copper seed layer over said layer of patterned dielectric material;

depositing a first layer of copper grains having a first initial grain size over said copper seed layer, said first layer of copper grains being deposited by an electroplating process; and

depositing a second layer of copper grains having a second initial grain size over said first layer of copper grains, said second layer of copper grains being deposited by an electroplating process.

2. The method of Claim 1 further comprising depositing at least one additional layer of copper grains of any initial grain size over said second layer of copper grains, said at least one additional layer of copper grains being deposited by an electroplating process.

3. The method of Claim 1 wherein said first initial grain size is smaller than said second initial grain size.

4. The method of Claim 2 wherein an initial grain size of said at least one additional layer of copper grains is larger than said first initial grain size.

5. The method of Claim 1 further comprising annealing said semiconductor wafer.

6. The method of Claim 5 wherein said annealing step is performed within a temperature range of 100° C to 300° C for a time between 10 minutes to 60 minutes.

7. A method of manufacturing copper interconnects on a semiconductor wafer comprising:

forming a layer of patterned dielectric material, said patterned dielectric material defining spaces for said copper interconnects;

depositing a copper seed layer over said layer of patterned dielectric material;

depositing a first layer of copper grains having a first initial grain size over said copper seed layer, said first layer of copper grains being deposited by an electroplating process; and

depositing at least one additional layer of copper grains of differing initial grain sizes over said first layer of copper grains, said at least one additional layer of copper grains being deposited by an electroplating process.

8. A method of manufacturing copper interconnects on a semiconductor wafer comprising:

forming a layer of patterned dielectric material, said patterned dielectric material defining spaces for said copper interconnects;

depositing a copper seed layer over said layer of patterned dielectric material;

depositing a first layer of copper grains having a first initial grain size over said copper seed layer, said first layer of copper grains being deposited by an electroplating process;

depositing a second layer of copper grains having a second initial grain size over said first layer of copper grains, said second layer of copper grains being deposited by an electroplating process and said second initial grain size being larger than said first initial grain size; and

annealing said semiconductor wafer.